74ALVC162334A

16-bit registered driver with inverted register enable and 30 Ω termination resistors (3-state)

Rev. 03 — 13 December 2006 Product data sheet

1. General description

The 74ALVC162334A is a 16-bit universal bus driver. Data flow is controlled by active LOW output enable ($\overline{OE}$), active LOW latch enable ($\overline{LE}$), and clock input (CP).

When $\overline{LE}$ is LOW, the A to Y data flow is transparent. When $\overline{LE}$ is HIGH and CP is held at LOW or HIGH, the data is latched; on the LOW to HIGH transient of CP, the A data is stored in the latch/flip-flop.

The 74ALVC162334A is designed with 30 Ω series resistors in both HIGH or LOW output stages.

When $\overline{OE}$ is LOW, the outputs are active. When $\overline{OE}$ is HIGH, the outputs go to the high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latch/flip-flop.

To ensure the high-impedance state during power-up or power-down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

2. Features

- Wide supply voltage range of 1.2 V to 3.6 V
- Complies with JEDEC standard 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive: ±24 mA at 3.0 V
- MULTIBYTE flow-through standard pinout architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Output drive capability 50 Ω transmission lines at 85 °C
- Integrated 30 Ω termination resistors
- Input diodes to accommodate strong drivers

3. Quick reference data

Table 1. Quick reference data

V_{CC} = 3.3 V ± 0.3 V; GND = 0 V; $t_r = t_f \leq$ 2.5 ns; C_L = 50 pF (see Figure 11).

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{PHL}	HIGH-to-LOW propagation delay	An to Yn; Figure 5		1.0	2.8	4.3	ns
		$\overline{LE}$ to Yn; Figure 6		1.3	2.8	4.4	ns
		CP to Yn; Figure 8		1.4	3.2	4.9	ns
t_{PLH}	LOW-to-HIGH propagation delay	An to Yn; Figure 5		1.0	2.8	4.3	ns
		$\overline{LE}$ to Yn; Figure 6		1.3	2.8	4.4	ns
		CP to Yn; Figure 8		1.4	3.2	4.9	ns
f_{max}	maximum input clock frequency	Figure 8		150	240	-	MHz
C_i	input capacitance			-	4.0	-	pF
C_{io}	input/output capacitance			-	8.0	-	pF
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC}	[2]				
		transparent mode; output enabled		-	10	-	pF
		transparent mode; output disabled		-	3	-	pF
		clocked mode; output enabled		-	21	-	pF
		clocked mode; output disabled		-	15	-	pF

[1] All typical values are at T_{amb} = 25 °C.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D) in μW.

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$, where:

f_i = input frequency in MHz;

C_L = output load capacitance in pF;

f_o = output frequency in MHz;

V_{CC} = supply voltage in V;

$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

4. Ordering information

Table 2. Ordering information

Type number	Temperature range	Package		
		Name	Description	Version
74ALVC162334ADGG	–40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

5. Functional diagram

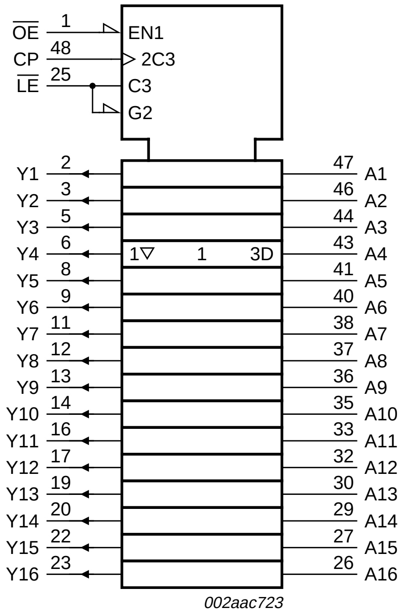


Fig 1. Logic symbol (IEEE/IEC)

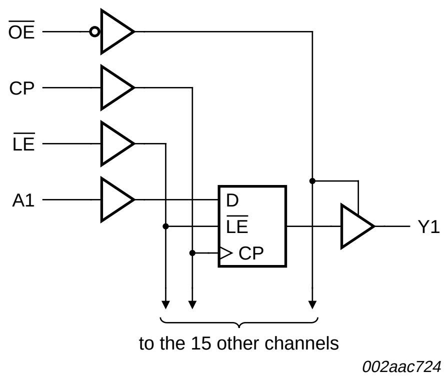


Fig 2. Logic diagram

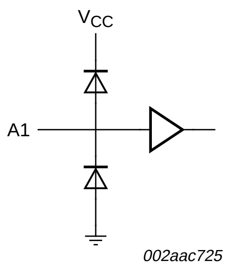


Fig 3. Typical input (data or control)

6. Pinning information

6.1 Pinning

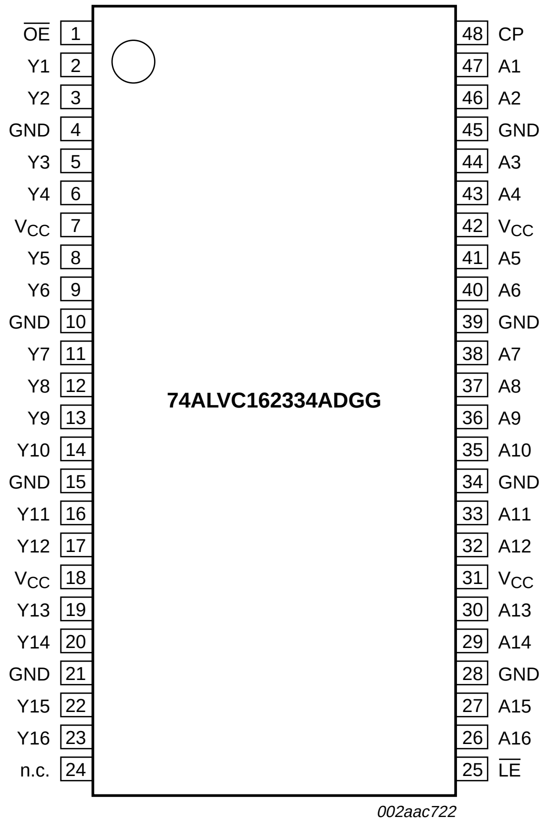


Fig 4. Pin configuration for TSSOP48

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$\overline{OE}$	1	output enable input (active LOW)
Y1	2	data output 1
Y2	3	data output 2
GND	4, 10, 15, 21, 28, 34, 39, 45	ground supply (0 V)
Y3	5	data output 3
Y4	6	data output 4
V_{CC}	7, 18, 31, 42	positive supply voltage
Y5	8	data output 5
Y6	9	data output 6
Y7	11	data output 7
Y8	12	data output 8

Table 3. Pin description *...continued*

Symbol	Pin	Description
Y9	13	data output 9
Y10	14	data output 10
Y11	16	data output 11
Y12	17	data output 12
Y13	19	data output 13
Y14	20	data output 14
Y15	22	data output 15
Y16	23	data output 16
n.c.	24	not connected
$\overline{LE}$	25	latch enable input (active LOW)
A16	26	data input 16
A15	27	data input 15
A14	29	data input 14
A13	30	data input 13
A12	32	data input 12
A11	33	data input 11
A10	35	data input 10
A9	36	data input 9
A8	37	data input 8
A7	38	data input 7
A6	40	data input 6
A5	41	data input 5
A4	43	data input 4
A3	44	data input 3
A2	46	data input 2
A1	47	data input 1
CP	48	clock input

7. Functional description

Refer to Figure 1 "Logic symbol (IEEE/IEC)" and Figure 2 "Logic diagram".

7.1 Function selection

Table 4. Function selection

H = HIGH voltage level; L = LOW voltage level; X = Don't care; Z = high-impedance OFF-state; ↑ = LOW to HIGH level transition.

Inputs				Outputs
$\overline{OE}$	$\overline{LE}$	CP	An	Yn
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	H	X	Y_0[1]
L	H	L	X	Y_0[2]

[1] Output level before the indicated steady-state input conditions were established, provided that CP is HIGH before $\overline{LE}$ goes LOW.

[2] Output level before the indicated steady-state input conditions were established.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V		-	–50	mA
V_I	input voltage		[1]	–0.5	+4.6	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage		[1]	–0.5	V_{CC} + 0.5	V
$I_{O(sink/source)}$	output sink or source current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	±100	mA
I_{GND}	ground current			-	±100	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}/pack	total power dissipation per package	for temperature range –40 °C to +125 °C; above +55 °C derate linearly with 8 mW/K		-	600	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	2.5 V range for maximum speed performance at 30 pF output load	2.3	-	2.7	V
		3.3 V range for maximum speed performance at 50 pF output load	3.0	-	3.6	V
		for low-voltage applications	1.2	-	3.6	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature	operating in free-air	–40	-	+85	°C
t_r	rise time	V_{CC} = 2.3 V to 3.0 V	0	-	20	ns/V
		V_{CC} = 3.0 V to 3.6 V	0	-	10	ns/V
t_f	fall time	V_{CC} = 2.3 V to 3.0 V	0	-	20	ns/V
		V_{CC} = 3.0 V to 3.6 V	0	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

T_{amb} = −40 °C to +85 °C; over recommended operating conditions; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IH}	HIGH-level input voltage	V_{CC} = 2.3 V to 2.7 V		1.7	1.2	-	V
		V_{CC} = 2.7 V to 3.6 V		2.0	1.5	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.3 V to 2.7 V		-	1.2	0.7	V
		V_{CC} = 2.7 V to 3.6 V		-	1.5	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		V_{CC} = 2.3 V to 3.6 V; I_O = −100 μA		V_{CC} − 0.2	V_{CC}	-	V
		V_{CC} = 2.3 V; I_O = −4 mA		V_{CC} − 0.4	V_{CC} − 0.11	-	V
		V_{CC} = 2.3 V; I_O = −6 mA		V_{CC} − 0.6	V_{CC} − 0.17	-	V
		V_{CC} = 2.7 V; I_O = −4 mA		V_{CC} − 0.5	V_{CC} − 0.09	-	V
		V_{CC} = 2.7 V; I_O = −8 mA		V_{CC} − 0.7	V_{CC} − 0.19	-	V
		V_{CC} = 3.0 V; I_O = −6 mA		V_{CC} − 0.6	V_{CC} − 0.13	-	V
		V_{CC} = 3.0 V; I_O = −12 mA		V_{CC} − 1.0	V_{CC} − 0.27	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		V_{CC} = 2.3 V to 3.6 V; I_O = 100 μA		-	GND	0.20	V
		V_{CC} = 2.3 V; I_O = 4 mA		-	0.07	0.40	V
		V_{CC} = 2.3 V; I_O = 6 mA		-	0.11	0.55	V
		V_{CC} = 2.7 V; I_O = 4 mA		-	0.06	0.40	V
		V_{CC} = 2.7 V; I_O = 8 mA		-	0.13	0.60	V
		V_{CC} = 3.0 V; I_O = 6 mA		-	0.09	0.55	V
		V_{CC} = 3.0 V; I_O = 12 mA		-	0.19	0.80	V
I_{LI}	input leakage current	V_{CC} = 2.3 V to 3.6 V; V_I = V_{CC} or GND		-	0.1	5	μA
I_{OZ}	off-state output current	3-state; V_{CC} = 2.3 V to 3.6 V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND		-	0.1	10	μA
I_{CC}	supply current	V_{CC} = 2.3 V to 3.6 V; V_I = V_{CC} or GND; I_O = 0 mA		-	0.2	40	μA
ΔI_{CC}	additional supply current	V_{CC} = 2.3 V to 3.6 V; V_I = V_{CC} − 0.6 V; I_O = 0 mA		-	150	750	μA
C_i	input capacitance			-	4.0	-	pF
C_{io}	input/output capacitance			-	8.0	-	pF
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC}	[2]				
		transparent mode; output enabled		-	10	-	pF
		transparent mode; output disabled		-	3	-	pF
		clocked mode; output enabled		-	21	-	pF
		clocked mode; output disabled		-	15	-	pF

[1] All typical values are at T_{amb} = 25 °C.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D) in μW.

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$, where:

f_i = input frequency in MHz;

C_L = output load capacitance in pF;
f_o = output frequency in MHz;
V_{CC} = supply voltage in V;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Dynamic characteristics

Table 8. Dynamic characteristics for V_{CC} = 2.3 V to 2.7 V range
V_{CC} = 2.3 V to 2.7 V; GND = 0 V; $t_r = t_f \leq 2.0$ ns; C_L = 30 pF (see Figure 11).

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{PHL}	HIGH-to-LOW propagation delay	An to Yn; Figure 5		1.0	3.5	5.0	ns
		$\overline{LE}$ to Yn; Figure 6		1.3	3.5	5.0	ns
		CP to Yn; Figure 8		1.4	3.7	5.4	ns
t_{PLH}	LOW-to-HIGH propagation delay	An to Yn; Figure 5		1.0	3.5	5.0	ns
		$\overline{LE}$ to Yn; Figure 6		1.3	3.5	5.0	ns
		CP to Yn; Figure 8		1.4	3.7	5.4	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{OE}$ to Yn; Figure 10	[2]	1.4	3.5	5.0	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{OE}$ to Yn; Figure 10	[2]	1.4	3.5	5.0	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{OE}$ to Yn; Figure 10	[3]	1.0	2.8	4.5	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{OE}$ to Yn; Figure 10	[3]	1.0	2.8	4.5	ns
t_W	pulse width	CP HIGH or LOW; Figure 8		3.3	1.0	-	ns
		$\overline{LE}$ HIGH; Figure 6		3.3	0.7	-	ns
t_{su}	set-up time	An to CP; Figure 9		1.0	-	-	ns
		An to $\overline{LE}$; Figure 7		1.5	-	-	ns
t_h	hold time	An to CP; Figure 9		0.4	0.4	-	ns
		An to $\overline{LE}$; Figure 7		1.4	0.4	-	ns
f_{max}	maximum input clock frequency	Figure 8		150	190	-	MHz

[1] All typical values are at V_{CC} = 2.5 V and T_{amb} = 25 °C.

[2] 3-state output enable time.

[3] 3-state output disable time.

Table 9. Dynamic characteristics for V_{CC} = 2.7 V
V_{CC} = 2.7 V; GND = 0 V; $t_r = t_f \leq 2.5$ ns; C_L = 50 pF (see Figure 11).

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{PHL}	HIGH-to-LOW propagation delay	An to Yn; Figure 5		1.0	3.3	4.6	ns
		$\overline{LE}$ to Yn; Figure 6		1.3	3.4	4.8	ns
		CP to Yn; Figure 8		1.4	3.8	6.2	ns
t_{PLH}	LOW-to-HIGH propagation delay	An to Yn; Figure 5		1.0	3.3	4.6	ns
		$\overline{LE}$ to Yn; Figure 6		1.3	3.4	4.8	ns
		CP to Yn; Figure 8		1.4	3.8	6.2	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{OE}$ to Yn; Figure 10	[2]	1.1	3.7	6.0	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{OE}$ to Yn; Figure 10	[2]	1.1	3.7	6.0	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{OE}$ to Yn; Figure 10	[3]	1.3	3.5	4.9	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{OE}$ to Yn; Figure 10	[3]	1.3	3.5	4.9	ns

Table 9. Dynamic characteristics for V_{CC} = 2.7 V *...continued*

V_{CC} = 2.7 V; GND = 0 V; $t_r = t_f \leq 2.5$ ns; C_L = 50 pF (see Figure 11).

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_w	pulse width	CP HIGH or LOW; Figure 8		3.3	1.2	-	ns
		$\overline{LE}$ HIGH; Figure 6		3.3	0.6	-	ns
t_{su}	set-up time	An to CP; Figure 9		1.0	-	-	ns
		An to $\overline{LE}$; Figure 7		1.5	-	-	ns
t_h	hold time	An to CP; Figure 9		0.6	0.3	-	ns
		An to $\overline{LE}$; Figure 7		1.7	0.4	-	ns
f_{max}	maximum input clock frequency	Figure 8		150	190	-	MHz

[1] All typical values are measured at T_{amb} = 25 °C.

[2] 3-state output enable time.

[3] 3-state output disable time.

Table 10. Dynamic characteristics for V_{CC} = 3.0 V to 3.6 V range

V_{CC} = 3.3 V ± 0.3 V; GND = 0 V; $t_r = t_f \leq 2.5$ ns; C_L = 50 pF (see Figure 11).

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{PHL}	HIGH-to-LOW propagation delay	An to Yn; Figure 5		1.0	2.8	4.3	ns
		$\overline{LE}$ to Yn; Figure 6		1.3	2.8	4.4	ns
		CP to Yn; Figure 8		1.4	3.2	4.9	ns
t_{PLH}	LOW-to-HIGH propagation delay	An to Yn; Figure 5		1.0	2.8	4.3	ns
		$\overline{LE}$ to Yn; Figure 6		1.3	2.8	4.4	ns
		CP to Yn; Figure 8		1.4	3.2	4.9	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{OE}$ to Yn; Figure 10	[2]	1.1	2.4	4.5	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{OE}$ to Yn; Figure 10	[2]	1.1	2.4	4.5	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{OE}$ to Yn; Figure 10	[3]	1.3	2.4	4.8	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{OE}$ to Yn; Figure 10	[3]	1.3	2.4	4.8	ns
t_w	pulse width	CP HIGH or LOW; Figure 8		3.3	0.7	-	ns
		$\overline{LE}$ HIGH; Figure 6		3.3	0.6	-	ns
t_{su}	set-up time	An to CP; Figure 9		1.0	-	-	ns
		An to $\overline{LE}$; Figure 7		1.5	-	-	ns
t_h	hold time	An to CP; Figure 9		0.9	0.3	-	ns
		An to $\overline{LE}$; Figure 7		1.4	0.4	-	ns
f_{max}	maximum input clock frequency	Figure 8		150	240	-	MHz

[1] All typical values are measured at V_{CC} = 3.3 V, T_{amb} = 25 °C.

[2] 3-state output enable time.

[3] 3-state output disable time.

11.1 AC waveforms

V_{CC} = 3.0 V to 3.6 V and V_{CC} = 2.7 V range:

V_M = 1.5 V; V_X = V_{OL} + 0.3 V; V_Y = V_{OH} – 0.3 V; V_I = 2.7 V.

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

V_{CC} = 2.3 V to 2.7 V and V_{CC} < 2.3 V range:

V_M = 0.5 V; V_X = V_{OL} + 0.15 V; V_Y = V_{OH} – 0.15 V; V_I = V_{CC}.

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

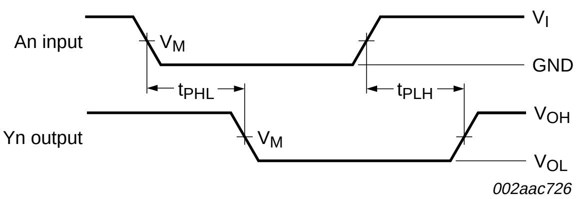


Fig 5. Input (An) to output (Yn) propagation delay

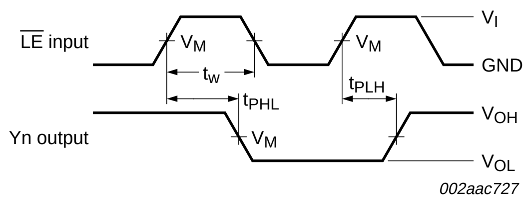
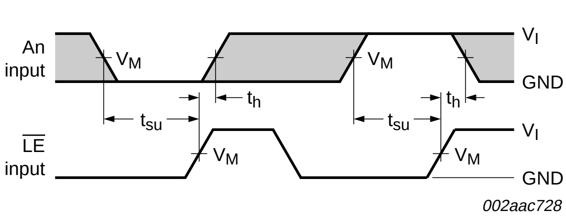


Fig 6. $\overline{LE}$ input pulse width, $\overline{LE}$ input to Yn output propagation delays



The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 7. Data set-up and hold times, An input to $\overline{LE}$ input

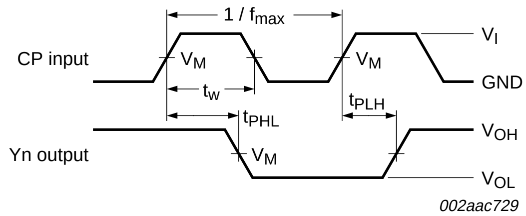
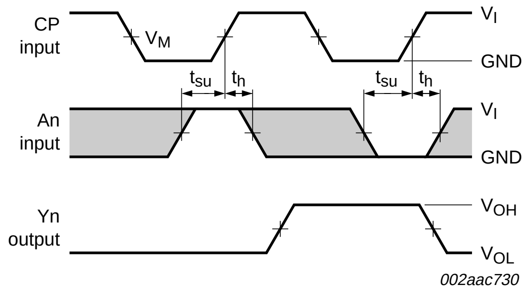


Fig 8. CP to Yn propagation delays, clock pulse width, and maximum clock frequency



The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 9. Data set-up and hold times, An input to CP input

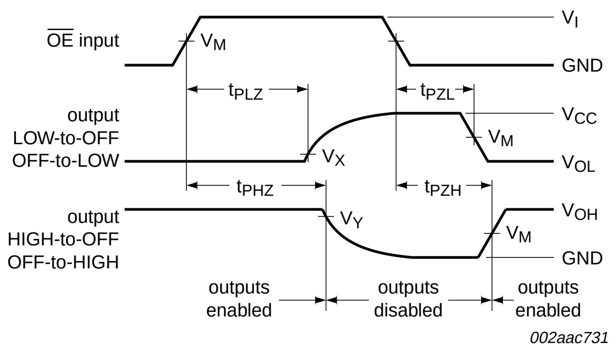
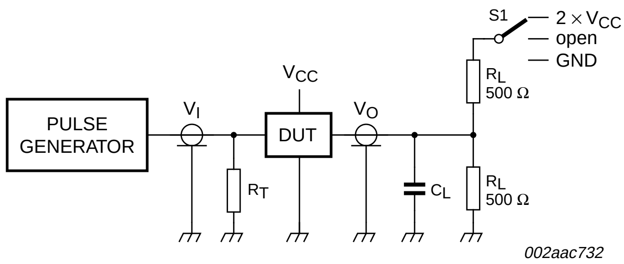


Fig 10. 3-state enable and disable times

12. Test information



Test data are given in Table 11.

R_L = load resistance.

C_L = load capacitance includes jig and probe capacitance.

R_T = termination resistance should be equal to Z_o of pulse generators.

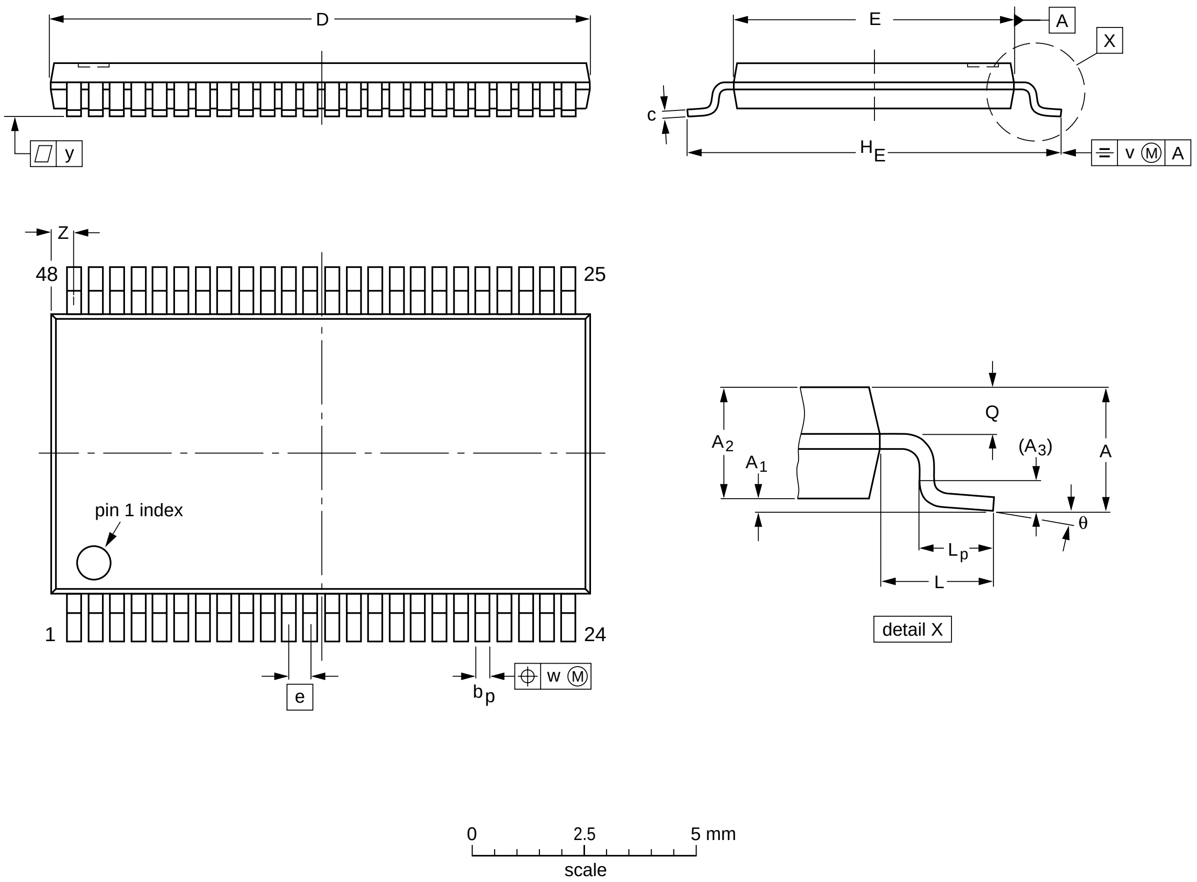
Fig 11. Test circuitry for switching times

Table 11. Test data

Supply voltage V_{CC}	Input		Load		Switch S1		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND (0 V)	2 × V_{CC}
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND (0 V)	2 × V_{CC}
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND (0 V)	2 × V_{CC}

13. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT362-1 (TSSOP48)

14. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 13) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 12 and 13

Table 12. SnPb eutectic process (from J-STD-020C)

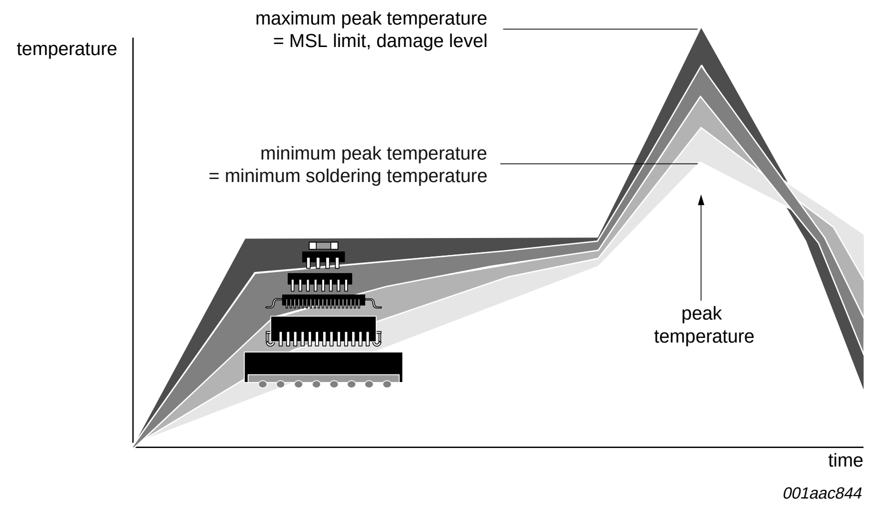
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 13. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 13.



MSL: Moisture Sensitivity Level

Fig 13. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

15. Abbreviations

Table 14. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
TTL	Transistor-Transistor Logic

16. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC162334A_3	20061213	Product data sheet	-	74ALVC162334A_2

Modifications:

- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.
- Legal texts have been adapted to the new company name where appropriate.
- Section 1 “General description”, 1st paragraph, 2nd sentence: changed “OE” to “$\overline{OE}$”
- Table 2 “Ordering information”: changed (SOT364-1; TSSOP56) package to (SOT362-1; TSSOP48) package
- Table 3 “Pin description” corrected:
  - changed “Y_1 to Y_{18}” to (Y1 to Y16, noted separately)
  - GND pins: added pins 4 and 39
  - V_{CC} pins changed from “7, 22, 35, 50” to “7, 18, 31, 42”
  - changed “A_1 to A_{18}” to (A1 to A16, noted separately)
- Figure 1 “Logic symbol (IEEE/IEC)”: corrected pin number for Y15 from “21” to “22”

Table 15. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications: (continued)	• Figure 1 "Logic symbol (IEEE/IEC)": corrected pin number for Y15 from "21" to "22" • Figure 2 "Logic diagram": – changed signal "A_0" to "A1" – changed signal "Y_0" to "Y1" – changed "to the 17 other channels" to "to the 15 other channels" • Table 5 "Limiting values" (title changed from "Absolute maximum ratings"): – parameter definition of I_{IK} changed from "DC input diode current" to "input clamping current" – parameter definition of I_{OK} changed from "DC output diode current" to "output clamping current" – symbol "I_O" (DC output source or sink current) changed to "$I_{O(sink/source)}$" (output sink or source current) – removed P_{tot}/pack information for SSOP package • Table 7 "Static characteristics" (title changed from "DC electrical characteristics"): – changed symbol "I_I" to "I_{LI}" – parameter definition of I_{OZ} changed from "3-State output OFF-state current" to "OFF-state output current" (moved "3-state" to Conditions column) – parameter definition of I_{CC} changed from "quiescent supply current" to "supply current" – parameter definition of ΔI_{CC} changed from "additional quiescent supply current" to "additional supply current" – added C_i, C_{io}, and C_{PD} parameters • Section 11 "Dynamic characteristics": table "AC characteristics for V_{CC} = 3.0 V to 3.6 V range and V_{CC} = 2.7 V" separated into 2 tables • Section 11.1 "AC waveforms": – 1st paragraph, 2nd line: changed "V_M = 1.5 V_{CC}" to "V_M = 1.5 V" – removed statement "V_M = 0.5V_{CC} at V_{CC} = 2.3 V to 2.7 V." from Figure 5, Figure 6, Figure 7, Figure 8, Figure 9 and Figure 10 as redundant (depends on voltage as stated above these figures) • Section 13 "Package outline": replaced SOT364-1 (TSSOP56) package outline drawing with Figure 12 "Package outline SOT362-1 (TSSOP48)"			
74ALVC162334A_2 (9397 750 07246)	20000620	Product specification	853-2197 23931	74ALVC162334A_1
74ALVC162334A_1 (9397 750 06963)	20000314	Product specification	853-2197 23314	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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